

ADAPTIVE VERSAL™ GEN1 & GEN2

VERSAL™ GEN1 & GEN2 ARCHITECTURE, TOOLS AND METHODOLOGY

TRAINING	PRICE	SESSIONS
VER_ARC Designing with Versal™ Gen1 & Gen2 : Architecture, Tools and Methodology (4 days)	3600 €	<ul style="list-style-type: none"> • October 12, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE

VERSAL™ GEN1 & GEN2 AI ENGINES

TRAINING	PRICE	SESSIONS
AIE_DSGN Designing with Versal™ AI Engine (AI, AIE-ML, AIE-MLv2) (4 days)	3600 €	<ul style="list-style-type: none"> • October 26, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE

VERSAL™ GEN1 & GEN2 CONNECTIVITY

TRAINING	PRICE	SESSIONS
VER_NOC Designing with the Network On Chip of AMD Versal™ (1 day)	1200 €	<ul style="list-style-type: none"> • May 13, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE
VER_TRX Designing with Versal™ Serial Transceivers (2 days)	2200 €	<ul style="list-style-type: none"> • September 17, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE
VER_PCIE Designing an Integrated PCI Express® System for Versal™ (2 days)	2200 €	<ul style="list-style-type: none"> • October 1, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE

EMBEDDED SOFTWARES

SOFTWARE DESIGN WITH THE VITIS TOOL

TRAINING	PRICE	SESSIONS
E_VITIS Software design of embedded systems with the Vitis™ tool (2 days)	2200 €	

SOFTWARE DESIGN WITH PETALINUX™

TRAINING	PRICE	SESSIONS
E_PLNX Embedded Design with AMD PetaLinux Tools (3 days)	3000 €	<ul style="list-style-type: none">• September 28, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE

ADAPTIVE SOCS

EMBEDDED DESIGN FOR AMD SOCS

TRAINING	PRICE	SESSIONS
E_ZAHS The essentials of embedded design for Xilinx Zynq™-7000, Zynq™ MPSoC and Versal™ components (4 days)	3600 €	<ul style="list-style-type: none">• November 23, 2026 Lieu : EN LIGNE ---- SESSION CONFIRMEE

VIVADO™ & FPGA

AMD VIVADO™ & VITIS HLS

TRAINING	PRICE	SESSIONS
D_HLS High-Level Synthesis with the Vitis Unified IDE (3 days)	3000 €	<ul style="list-style-type: none"> September 14, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE
F_VBASE Designing FPGAs Using the Vivado™ (4 days)	3600 €	
F_STAXDC Static Timing Analysis (STA), Xilinx Design Constraints (XDC) and Advanced use of Vivado™ (4 days)	3600 €	<ul style="list-style-type: none"> May 26, 2026 Lieu : EN LIGNE ---- SESSION CONFIRMEE <ul style="list-style-type: none"> December 7, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE
F_DFX Designing with Dynamic Function eXchange (DFX) Using the Vivado™ (3 days)	3000 €	

FPGA ARCHITECTURES

TRAINING	PRICE	SESSIONS
F_SU Designing with the AMD UltraScale+™ Families (Spartan™ included) (2 days)	2200 €	<ul style="list-style-type: none"> May 11, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE

FPGA CONNECTIVITIES

TRAINING	PRICE	SESSIONS
C_TRX Designing with Serial Transceivers (2 days)	On site and/or according to requests	
C_PCIE Designing an Integrated PCI Express System (2 days)	2200 €	

DIGITAL SIGNAL PROCESSING ON RFSOC AND FPGA

DESIGN WITH THE ZYNQ™ ULTRASCALE+ RFSOC

TRAINING	PRICE	SESSIONS
C_RFSOC Design with the Zynq™ UltraScale+ RFSoc (3 days)		On site and/or according to requests

DIGITAL SIGNAL PROCESSING ON FPGA

TRAINING	PRICE	SESSIONS
D_ESS Essential DSP implementation techniques for AMD FPGAs (2 days)		On site and/or according to requests

HDL LANGUAGES

VHDL

TRAINING	PRICE	SESSIONS
L_VHDL VHDL Logical Synthesis and Simulation for AMD FPGA design (5 days)	4400 €	<ul style="list-style-type: none"> • June 22, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE • December 14, 2026 Lieu : EN LIGNE ---- CONFIRMATION EN ATTENTE

UPGRADING VHDL TO VERILOG AND VERILOG TO VHDL

TRAINING	PRICE	SESSIONS
L_VV_UP Upgrading VHDL to Verilog and Verilog to VHDL (2 days)	2200 €	