

Training Program

Ref:L VV UP - 09/27/2025



Upgrading VHDL to Verilog and Verilog to VHDL

COURSE DURATION



2 days - 14 hours

TARGET OBJECTIVES AND SKILLS

- 1 Know the instruction sets for RTL synthesis and grasp the differences and the multiple possibilities offered by the VHDL and Verilog languages
- 2 Know the instruction sets for the simulation and grasp the differences and the multiple possibilities offered by the VHDL and Verilog languages

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.



PREREQUISITES

 This course is intended for electronic engineers who already have a good knowledge of digital electronic circuit design, and who master one of the RTL logic synthesis languages (VHDL or Verilog), and who wish to acquire additional knowledge of the second RTL logic synthesis language (VHDL or Verilog).

NOTES

• Release date: 15/11/2024



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COURSE CONTENT

DAY 1

- Objective 1
 - Rules for writing VHDL/Verilog code in logical synthesis
 - Concept of entity/architecture
 - Predefined objects and types
 - Competing Instructions
 - Sequential instructions
 - Hierarchy management for better reuse
 - Notions of variables and examples of use
 - Generality and automatic parameterization of reusable

modules

- Predefined Attributes Useful in Logical Synthesis
- Functions and procedures
- Definition of packages and libraries

DAY 2

- Objective 2
 - Testbenches and simulation
 - Some basic rules for writing an efficient testbench
 - Simulation-specific instructions
 - Writing component models to make simulation more realistic
 - Writing and reading ASCII files
 - Generation of information messages

TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- Teaching methods:
 - Alternating lectures, technical questionnaires and exercises on individual machines.
- Pedagogical follow-up:
 - Signed attendance sheet
- Pedagogical assessment :
 - o Continuous assessment and progress sheet :
 - Technical questionnaire
 - Practical work results
 - Validation of objectives
- Satisfaction survey :
 - At the end of training: assessment form completed by the trainee
 - At 3 months: evaluation form completed by the trainee after application to the company
- Certificate:
 - Training certificate with assessment of learning provided to trainee
 - o Certificate of completion provided to employer



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TEACHING METHODS

• Inter-company online training :

- o Fast Internet connection, webcam, headset
- Presentation by Webex by Cisco



- o Provision of course material in PDF format
- Labs on individual Cloud PC by RealVNC

GREALVIC

Intra-company face-to-face training on customer site (details to be confirmed prior to training)

- Suggested supply by the customer :
 - Training room
 - Video projector
 - Whiteboard
 - Individual PC with AMD tools
- o Provided by MVD Training :
 - Course material in PDF format
 - Practical work on individual PCs (loan of equipment available on request)

RECOMMENDED COMPUTER HARDWARE

• Inter-company online training:

- Recent computer OS Linux or Windows 64-bits
- o Fast Internet, webcam, headset
- Software tool WebEx Cisco
- AMD remote tools :
 - Software tool RealVNC Viewer
- AMD local tools :
 - Software tool AMD Vivado 2022.2

• Face-to-face training on customer site :

- Recent computer OS Linux or Windows 64-bits
- o Software tool AMD Vivado 2022.2

TEACHING STAFF

• William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :

- Expert AMD FPGA Language VHDL/Verilog RTL Design
- Expert AMD SoC & MPSoC Language C/C++ System Design
- o Expert DSP & AMD RFSoC HLS Matlab Design DSP RF
- o Expert AMD Versal Al Engines Heteregenous System Architect

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

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