VHDL Logical Synthesis and Simulation for AMD FPGA design

5 days - 35 hours

OBJECTIVES

- After completing this training, you will have the skills to:
  - 1 - Understand the architecture of a Series-7 FPGA
  - 2 - Understand the multiple possibilities offered by the VHDL language and understand the concepts of logic synthesis
  - 3 - Know the writing styles and their impact on the quality of the synthesis results
  - 4 - Handle development tools and implementation reports
  - 5 - Understand the multiple simulation possibilities offered by the VHDL language and build efficient testbenches

PREREQUISITES

- This training is intended to electronic engineers who already have a good knowledge in designing digital electronic circuits, who are willing to acquire a strong designing methodology, and to take the best of VHDL language and the associated synthesis and simulation tools for designing AMD FPGA.

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 13/12/2021

CHAPTERS

DAY 1

- Objective 1
  - CLB and slices notion
  - Dedicated RAM blocks and use modes
  - Dedicated multipliers and DSP48 blocks
  - In/Out blocks
  - Clocks distribution, MMCMs and PLLs
  - Configuration

DAY 2

- Objective 2
  - Notion of entity / architecture
  - Concurrent and sequential instructions
  - Predefined types and objects
  - Predefined operators and of use extended by using standardized packages
  - Concurrent instructions : when, with select, for generate

DAY 3

- Objective 2
  - Process
  - Organization of design by functional modules
  - Inference and instancing notions
  - Precautions for an evolutionary and / or re-usable code

DAY 4

- Objective 3
  - Notion of variable and example of use
  - Genericity and automatic configuration of re-usable modules
  - Useful predefined attributes in logical synthesis
  - Functions and procedures
  - Definition of packages and libraries
- Objective 4
  - Synchronous design
  - Static timing analysis
  - Implementation and tuning tools

DAY 5

- Objective 5
  - VHDL instructions specific to simulation
  - Writing components models intended to make the simulation more realistic
  - Use of existing models and simulation packages
  - Writing and reading of ASCII files
  - Generating information messages

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vivado Design Suite 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

Administratif / Formateur : (+33) 06 74 52 37 89
info@mvd-training.com

Qualiopi processus certifié
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La certification a été délivrée au titre de la catégorie d'action suivante :
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