VHDL Logical Synthesis and Simulation for AMD FPGA design

COURSE DURATION

5 days - 35 hours

TARGET OBJECTIVES AND SKILLS

- 1 - Understand the architecture of a Series-7 FPGA
- 2 - Understand the multiple possibilities offered by the VHDL language and understand the concepts of logic synthesis
- 3 - Know the writing styles and their impact on the quality of the synthesis results
- 4 - Handle development tools and implementation reports
- 5 - Understand the multiple simulation possibilities offered by the VHDL language and build efficient testbenches

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.

PREREQUISITES

- This training is intended to electronic engineers who already have a good knowledge in designing digital electronic circuits, who are willing to acquire a strong designing methodology, and to take the best of VHDL language and the associated synthesis and simulation tools for designing AMD FPGA.

NOTES

- Release date: 15/11/2024

COURSE CONTENT

DAY 1

- Objective 1
  - CLB and slices notion
  - Dedicated RAM blocks and use modes
  - Dedicated multipliers and DSP48 blocks
  - In/Out blocks
  - Clocks distribution, MMCMs and PLLs
  - Configuration

DAY 2

- Objective 2
  - Notion of entity / architecture
  - Concurrent and sequential instructions
  - Predefined types and objects
  - Predefined operators and of use extended by using standardized packages
  - Concurrent instructions : when, with select, for generate

DAY 3

- Objective 2
  - Process
  - Organization of design by functional modules
  - Inference and instancing notions
  - Precautions for an evolutionary and / or re-usable code

DAY 4

- Objective 3
  - Notion of variable and example of use
  - Genericity and automatic configuration of re-usable modules
  - Useful predefined attributes in logical synthesis
  - Functions and procedures
  - Definition of packages and libraries
- Objective 4
  - Synchronous design
  - Static timing analysis
  - Implementation and tuning tools

DAY 5

- Objective 5
  - VHDL instructions specific to simulation
  - Writing components models intended to make the simulation more realistic
  - Use of existing models and simulation packages
  - Writing and reading of ASCII files
  - Generating information messages

TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- **Teaching methods :**
  - Alternating lectures, technical questionnaires and exercises on individual machines.
- **Pedagogical follow-up :**
  - Signed attendance sheet
- **Pedagogical assessment :**
  - Continuous assessment and progress sheet :
    - Technical questionnaire
    - Practical work results
    - Validation of objectives
- **Satisfaction survey :**
  - At the end of training: assessment form completed by the trainee
  - At 3 months: evaluation form completed by the trainee after application to the company
- **Certificate :**
  - Training certificate with assessment of learning provided to trainee
  - Certificate of completion provided to employer

TEACHING METHODS

- **Inter-company online training :**
  - Fast Internet connection, webcam, headset
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on individual Cloud PC by RealVNC
- **Intra-company face-to-face training on customer site : (details to be confirmed prior to training)**
  - Suggested supply by the customer :
    - Training room
    - Video projector
    - Whiteboard
    - Individual PC with AMD tools
  - Provided by MVD Training :
    - Course material in PDF format
    - Practical work on individual PCs (loan of equipment available on request)

RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
  - Recent computer OS Linux or Windows 64-bits
  - Fast Internet, webcam, headset
  - Software tool WebEx Cisco
  - ***AMD remote tools :***
    - Software tool RealVNC Viewer
  - ***AMD local tools :***
    - Software tool AMD Vivado
- **Face-to-face training on customer site :**
  - Recent computer OS Linux or Windows 64-bits
  - Software tool AMD Vivado

TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

William DULUC, 06 74 52 37 89, info@mvd-training.com