

Designing FPGAs Using the Vivado™

GENERAL OBJECTIVE OF THE TRAINING

Designing an FPGA design, which includes creating a Vivado™ Design Suite project with source files, simulating the design, performing pin assignments, applying basic timing constraints, synthesizing, implementing, and debugging the design.

COURSE DURATION



4 days - 28 hours

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to discuss your requirements.



PREREQUISITES

- Basic knowledge of the VHDL or Verilog language
- Digital design knowledge

NOTES

- Release date: 15/11/2024

TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
 - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
 - Expert AMD SoC & MPSoC - Language C/C++ - System Design
 - Expert DSP & AMD RFSoc - HLS - Matlab - Design DSP RF
 - Expert AMD Versal - AI Engines - Heterogenous System Architect

TARGET OBJECTIVES AND SKILLS

- 1 - Use the Vivado IDE I/O Planning layout to perform pin assignments
- 2 - Describe the supported design flows of the Vivado IDE
- 3 - Synthesize and implement the HDL design, and generate a DRC report to detect and fix design issues
- 4 - Create and package your own IP and use the Vivado IP integrator to create a block design
- 5 - Describe how power analysis and optimization is performed
- 6 - Apply clock, I/O timing and timing exception constraints and perform timing analysis
- 7 - Identify synchronous design techniques
- 8 - Describe how the FPGA is programmed
- 9 - Use the Vivado logic analyzer and debug cores to debug a design

COURSE CONTENT

DAY 1

- Objective 1
 - Introduction to Vivado Design Flows {Lecture}
 - Introduction to FPGA Architecture, 3D IC, SoC {Lecture}
 - UltraFast Design Methodology: Planning {Lecture}
 - Vivado Design Suite I/O Pin Planning {Lecture, Lab}
- Objective 2
 - Vivado Design Suite Project Mode {Lecture, Lab}
 - Scripting in Vivado Design Suite Project Mode {Lecture}
 - HDL Coding Techniques {Lecture}
 - Inference {Lecture}
 - Simulation {Lecture, Lab}
- Objective 3
 - Synthesis and Implementation {Lecture, Lab}
 - Introduction to Vivado Reports {Lecture, Labs}

DAY 2

- Objective 4
 - Vivado IP Flow {Lecture, Lab}
 - Creating and Packaging Custom IP {Lecture, Lab}
 - Using an IP Container {Lecture}
 - Designing with IP Integrator {Lecture, Lab}
- Objective 5
 - Power Analysis and Optimization Using the Vivado Design Suite {Lecture}
- Objective 6
 - Baselineing {Lecture}
 - Timing Constraints Editor {Lecture}
 - Timing Summary Report {Lecture}

- Clocking Resources {Lecture}
- Introduction to Clock Constraints {Lecture}



DAY 3

- Objective 6
 - Generated Clocks {Lecture, Lab}
 - Report Clock Networks {Lecture}
 - Clock Group Constraints {Lecture}
 - Report Clock Interaction {Lecture}
 - Setup and Hold Timing Analysis {Lecture}
 - I/O Logic Resources {Lecture}
 - I/O Constraints and Virtual Clocks {Lecture, Lab}
 - Timing Constraints Wizard {Lecture}
 - Introduction to Timing Exceptions {Lecture, Lab}
- Objective 7
 - Synchronous Design Techniques {Lecture}
 - Synchronization Circuits {Lecture}
 - Timing Constraints Priority {Lecture}

DAY 4

- Objective 8
 - Introduction to FPGA Configuration {Lecture}
 - Configuration Process {Lecture}
 - Configuration Modes {Lecture}
 - Daisy Chains and Gangs in Configuration {Lecture}
 - Bitstream Security {Lecture}
- Objective 9
 - Introduction to the Vivado Logic Analyzer {Lecture}
 - Introduction to Triggering {Lecture}
 - Debug Cores {Lecture}
 - HDL Instantiation Debug Probing Flow {Lecture, Lab}
 - Netlist Insertion Debug Probing Flow {Lecture, Lab}
 - Debug Flow in an IP Integrator Block Design {Lecture, Lab}

TEACHING METHODS

- **Inter-company online training :**
 - Fast Internet connection, webcam, headset
 - Presentation by Webex by Cisco

 - Provision of course material in PDF format
 - Labs on individual Cloud PC by RealVNC

- **Intra-company face-to-face training on customer site : (details to be confirmed prior to training)**
 - Suggested supply by the customer :
 - Training room
 - Video projector
 - Whiteboard
 - Individual PC with AMD tools
 - Provided by MVD Training :
 - Course material in PDF format
 - Practical work on individual PCs (loan of equipment available on request)

RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
 - Recent computer OS Linux or Windows 64-bits
 - Fast Internet, webcam, headset
 - Software tool WebEx Cisco
 - **AMD remote tools :**
 - Software tool RealVNC Viewer
 - **AMD local tools :**
 - Software tool AMD Vivado 2022.2
- **Face-to-face training on customer site :**
 - Recent computer OS Linux or Windows 64-bits
 - Software tool AMD Vivado 2022.2

TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- **Teaching methods :**
 - Alternating lectures, technical questionnaires and exercises on individual machines.
- **Pedagogical follow-up :**
 - Signed attendance sheet
- **Pedagogical assessment :**
 - Continuous assessment and progress sheet :
 - Technical questionnaire
 - Practical work results
 - Validation of objectives
- **Satisfaction survey :**
 - At the end of training: assessment form completed by the trainee
 - At 3 months: evaluation form completed by the trainee after application to the company
- **Certificate :**
 - Training certificate with assessment of learning provided to trainee
 - Certificate of completion provided to employer

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

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