Designing with the AMD UltraScale+™ Families (Spartan™ included)

COURSE DURATION

2 days - 14 hours

TARGET OBJECTIVES AND SKILLS

- 1 - Describe the key features and fundamental blocks and the impact they have on your HDL coding style
- 2 - Describe the various on-chip memory and DSP resources available
- 3 - Utilize the advanced I/O capabilities for various connectivity needs
- 4 - Describe clocking, including buffer types, clock management tiles, and routing for enhanced timing
- 5 - Identify the high-speed transceivers for use in applications such as PCIe® Gen4
- 6 - Explain the configuration process for UltraScale+™ devices
- 7 - Know how to effectively migrate your IP and design to the UltraScale+™ architecture and leverage the Power Design Manager (PDM) tool for power estimation.

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.

PREREQUISITES

- Basic knowledge FPGAs architectures
- A successful first experience of designing an VHDL–based FPGA using Vivado™ Design Suite

NOTES

- Release date: 19/09/2025

COURSE CONTENT

DAY 1

- Objective 1
  - Introduction to the UltraScale+™ Families {Lecture}
  - Introduction to the Spartan™ UltraScale+™ Architecture {Lecture}
  - Programmable Logic {Lecture}
  - HDL Coding Techniques {Lecture}
- Objective 2
  - Block RAM Memory Resources {Lecture}
  - FIFO Memory Resources {Lecture}
  - UltraRAM Memory Resources {Lecture}
  - DSP Resources {Lecture}
- Objective 3
  - UltraScale Architecture I/O Resources Overview {Lecture}
  - I/O Resources – Component Mode {Lecture}
  - I/O Resources – Native Mode {Lecture}

DAY 2

- Objective 4
  - Clocking Resources {Lectures}
- Objective 5
  - Architecture Transceivers {Lecture}
  - PCI Express® {Lecture}
- Objective 6
  - Spartan™ UltraScale+™ FPGA configuration & security {Lecture}
- Objective 7
  - FPGA design migration {Lecture}
  - Power Design Manager {Lecture}

TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- **Teaching methods :**
  - Alternating lectures, technical questionnaires and exercises on individual machines.
- **Pedagogical follow-up :**
  - Signed attendance sheet
- **Pedagogical assessment :**
  - Continuous assessment and progress sheet :
    - Technical questionnaire
    - Practical work results
    - Validation of objectives
- **Satisfaction survey :**
  - At the end of training: assessment form completed by the trainee
  - At 3 months: evaluation form completed by the trainee after application to the company
- **Certificate :**
  - Training certificate with assessment of learning provided to trainee
  - Certificate of completion provided to employer

TEACHING METHODS

- **Inter-company online training :**
  - Fast Internet connection, webcam, headset
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on individual Cloud PC by RealVNC
- **Intra-company face-to-face training on customer site : (details to be confirmed prior to training)**
  - Suggested supply by the customer :
    - Training room
    - Video projector
    - Whiteboard
    - Individual PC with AMD tools
  - Provided by MVD Training :
    - Course material in PDF format
    - Practical work on individual PCs (loan of equipment available on request)

RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
  - Recent computer OS Linux or Windows 64-bits
  - Fast Internet, webcam, headset
  - Software tool WebEx Cisco
  - ***AMD remote tools :***
    - Software tool RealVNC Viewer
  - ***AMD local tools :***
    - Software tool AMD Vivado
- **Face-to-face training on customer site :**
  - Recent computer OS Linux or Windows 64-bits
  - Software tool AMD Vivado

TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

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