# Static Timing Analysis (STA), Xilinx Design Constraints (XDC) and Advanced use of Vivado™

## COURSE DURATION

4 days - 28 hours

## TARGET OBJECTIVES AND SKILLS

- 1 - Optimize HDL code to maximize FPGA resources and performance and use the UltraFast™ design methodology.
- 2 - Master the Vivado tool, apply timing constraints (XDC) and use appropriate timing reports.
- 3 - Identify key areas to optimize your design, minimize metastability issues and make your reset in your system more reliable
- 4 - Apply timing constraints on inputs/outputs to achieve performance targets
- 5 - Use advanced implementation options, such as incremental build flow, physical optimization techniques and re-entrant mode
- 6 - Use advanced techniques to improve design performance
- 7 - Debug a design during the start-up phase and use advanced debugging functions

## CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.

## PREREQUISITES

- Intermediate knowledge in HDL language (VHDL or Verilog)
- Experience with the Vivado™ Design suite and FPGAs.

## NOTES

- Release date: 15/11/2024

## COURSE CONTENT

**DAY 1**

- Objective 1
  - Introduction to FPGA architecture and Static Timing Analysis (STA) {Lectures}
  - HDL coding techniques {Lecture}
  - Ultra-fast design methodology: Board planning and design creation {Lectures}
- Objective 2
  - Flow of the Vivado Design software suite {Lectures, Lab}
  - Vivado synthesis and implementation {Lecture}
  - Introduction to Vivado reports {Lecture}

**DAY 2**

- Objective 2
  - Baselining {Lecture}
  - Timing Constraints Editor {Lecture}
  - Clocking Resources {Lecture}
  - Introduction to Clock Constraints {Lecture}
  - Generated Clocks {Lecture, Lab}
  - Clock Group Constraints {Lecture}
  - Report Clock Interaction {Lecture}
  - Timing Summary Report {Lecture}
  - Setup and Hold Timing Analysis {Lecture}
  - I/O Constraints and Virtual Clocks {Lecture, Lab}
  - Introduction to Timing Exceptions {Lecture, Lab}

**DAY 3**

- Objective 3
  - Synchronous Design Techniques {Lecture}
  - Synchronization Circuits {Lecture, Lab}
  - Resets {Lecture}
  - Register Duplication {Lecture}
- Objective 4
  - I/O Timing Scenarios {Lecture}
  - System-Synchronous I/O Timing {Lecture}
  - Source-Synchronous I/O Timing {Lecture, Lab}
  - I/O Logic Resources {Lecture}
  - Report Datasheet {Lecture}
  - Timing Constraints Priority {Lecture}
- Objective 5
  - UltraFast Design Methodology: Implementation {Lecture}
  - Timing Closure Using Physical Optimization Techniques {Lecture}
  - Incremental Compile Flow {Lecture}

**DAY 4**

- Objective 6
  - QoR Reports Overview {Lecture, Lab}
  - Reducing Logic Delay {Lecture}
  - Reducing Net Delay {Lecture}
  - Improving Clock Skew {Lecture}
  - Improving Clock Uncertainty {Lecture, Lab}
  - Intelligent Design Runs (IDR) {Lecture, Lab}
  - Introduction to Floorplanning {Lecture}
- Objective 7
  - Vivado Design Suite ECO Flow {Lecture, Lab}
  - JTAG to AXI Master Core {Lecture}
  - Trigger and Debug at Device Startup {Lecture}
  - Trigger Using the Trigger State Machine in the Vivado Logic Analyzer {Lecture, Lab}

## TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- **Teaching methods :**
  - Alternating lectures, technical questionnaires and exercises on individual machines.
- **Pedagogical follow-up :**
  - Signed attendance sheet
- **Pedagogical assessment :**
  - Continuous assessment and progress sheet :
    - Technical questionnaire
    - Practical work results
    - Validation of objectives
- **Satisfaction survey :**
  - At the end of training: assessment form completed by the trainee
  - At 3 months: evaluation form completed by the trainee after application to the company
- **Certificate :**
  - Training certificate with assessment of learning provided to trainee
  - Certificate of completion provided to employer

## TEACHING METHODS

- **Inter-company online training :**
  - Fast Internet connection, webcam, headset
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on individual Cloud PC by RealVNC
- **Intra-company face-to-face training on customer site : (details to be confirmed prior to training)**
  - Suggested supply by the customer :
    - Training room
    - Video projector
    - Whiteboard
    - Individual PC with AMD tools
  - Provided by MVD Training :
    - Course material in PDF format
    - Practical work on individual PCs (loan of equipment available on request)

## RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
  - Recent computer OS Linux or Windows 64-bits
  - Fast Internet, webcam, headset
  - Software tool WebEx Cisco
  - ***AMD remote tools :***
    - Software tool RealVNC Viewer
  - ***AMD local tools :***
    - Software tool AMD Vivado 2022.2
- **Face-to-face training on customer site :**
  - Recent computer OS Linux or Windows 64-bits
  - Software tool AMD Vivado 2022.2

## TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

## TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

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