Designing with Dynamic Function eXchange (DFX) Using the Vivado™

COURSE DURATION

3 days - 21 hours

TARGET OBJECTIVES AND SKILLS

- 1 - Describe Dynamic Function eXchange and the DFX tool flow with Vivado.
- 2 - Identify how Dynamic Function eXchange allocates various resources for AMD components.
- 3 - Implementing and debugging a Dynamic Function eXchange system.
- 4 - Implement a DFX system in an embedded environment using the Vitis IDE.
- 5 - Generating the appropriate full and partial bitstreams for a DFX design.
- 6 - Use advanced functions to create a DFX design.

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.

PREREQUISITES

- Designing FPGAs with Vivado™
- Working HDL knowledge (VHDL or Verilog)

NOTES

- Release date: 14/02/2025

COURSE CONTENT

DAY 1

- Objective 1
  - Introduction to Dynamic Function eXchange (DFX) {Lecture}
  - DFX Flow Using the Vivado Design Suite GUI {Lecture, Lab}
  - DFX Flow Using Vivado Design Suite Tcl Commands {Lecture, Lab}
- Objective 2
  - DFX Design Considerations for All Xilinx Devices {Lecture}
  - DFX Design Considerations for 7 Series, Zynq SoC, UltraScale, and UltraScale+ Devices {Lecture}
  - DFX Design Considerations for Versal Devices {Lecture}

DAY 2

- Objective 3
  - Floorplanning a DFX Design {Lecture, Lab}
  - DFX Timing Analysis and Constraints {Lecture, Lab}
  - DFX Debugging {Lecture, Lab}
- Objective 4
  - DFX in Embedded Systems {Lecture, Lab}
  - DFX Designs Using the PCIe Core {Lecture}
- Objective 5
  - Configuring Devices Using DFX {Lecture}
  - Configuration Parameters {Lecture}
  - DFX Bitstreams {Lecture}
  - DFX Bitstream Integrity {Lecture}

DAY 3

- Objective 6
  - DFX Intellectual Property (IP) {Lecture, Lab}
  - DFX Block Design Containers in IP Integrator {Lecture, Lab}
  - Abstract Shell for Dynamic Function eXchange {Lecture, Lab}
  - Nested DFX {Lecture, Lab}

TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- **Teaching methods :**
  - Alternating lectures, technical questionnaires and exercises on individual machines.
- **Pedagogical follow-up :**
  - Signed attendance sheet
- **Pedagogical assessment :**
  - Continuous assessment and progress sheet :
    - Technical questionnaire
    - Practical work results
    - Validation of objectives
- **Satisfaction survey :**
  - At the end of training: assessment form completed by the trainee
  - At 3 months: evaluation form completed by the trainee after application to the company
- **Certificate :**
  - Training certificate with assessment of learning provided to trainee
  - Certificate of completion provided to employer

TEACHING METHODS

- **Inter-company online training :**
  - Fast Internet connection, webcam, headset
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on individual Cloud PC by RealVNC
- **Intra-company face-to-face training on customer site : (details to be confirmed prior to training)**
  - Suggested supply by the customer :
    - Training room
    - Video projector
    - Whiteboard
    - Individual PC with AMD tools
  - Provided by MVD Training :
    - Course material in PDF format
    - Practical work on individual PCs (loan of equipment available on request)

RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
  - Recent computer OS Linux or Windows 64-bits
  - Fast Internet, webcam, headset
  - Software tool WebEx Cisco
  - ***AMD remote tools :***
    - Software tool RealVNC Viewer
  - ***AMD local tools :***
    - Software tool AMD Vivado 2022.2
- **Face-to-face training on customer site :**
  - Recent computer OS Linux or Windows 64-bits
  - Software tool AMD Vivado 2022.2

TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

William DULUC, 06 74 52 37 89, info@mvd-training.com