Static Timing Analysis (STA), Xilinx Design Constraints (XDC) and Advanced use of Vivado™

4 days - 28 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1 - Optimize HDL code to maximize FPGA resources and performance and use the UltraFast™ design methodology.
  - 2 - Master the Vivado tool, apply timing constraints (XDC) and use appropriate timing reports.
  - 3 - Identify key areas to optimize your design, minimize metastability issues and make your reset in your system more reliable
  - 4 - Apply timing constraints on inputs/outputs to achieve performance targets
  - 5 - Use advanced implementation options, such as incremental build flow, physical optimization techniques and re-entrant mode
  - 6 - Use advanced techniques to improve design performance
  - 7 - Debug a design during the start-up phase and use advanced debugging functions

PREREQUISITES

- Intermediate knowledge in HDL language and a first experience with the Vivado™ Design suite and FPGAs.

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 17/09/2023

CHAPTERS

DAY 1

- Objective 1
  - Introduction to FPGA architecture and Static Timing Analysis (STA) {Lectures}
  - HDL coding techniques {Lecture}
  - Ultra-fast design methodology: Board planning and design creation {Lectures}
- Objective 2
  - Flow of the Vivado Design software suite {Lectures, Lab}
  - Vivado synthesis and implementation {Lecture}
  - Introduction to Vivado reports {Lecture}

DAY 2

- Objective 2
  - Baselining {Lecture}
  - Timing Constraints Editor {Lecture}
  - Clocking Resources {Lecture}
  - Introduction to Clock Constraints {Lecture}
  - Generated Clocks {Lecture, Lab}
  - Clock Group Constraints {Lecture}
  - Report Clock Interaction {Lecture}
  - Timing Summary Report {Lecture}
  - Setup and Hold Timing Analysis {Lecture}
  - I/O Constraints and Virtual Clocks {Lecture, Lab}
  - Introduction to Timing Exceptions {Lecture, Lab}

DAY 3

- Objective 3
  - Synchronous Design Techniques {Lecture}
  - Synchronization Circuits {Lecture, Lab}
  - Resets {Lecture}
  - Register Duplication {Lecture}
- Objective 4
  - I/O Timing Scenarios {Lecture}
  - System-Synchronous I/O Timing {Lecture}
  - Source-Synchronous I/O Timing {Lecture, Lab}
  - I/O Logic Resources {Lecture}
  - Report Datasheet {Lecture}
  - Timing Constraints Priority {Lecture}
- Objective 5
  - UltraFast Design Methodology: Implementation {Lecture}
  - Timing Closure Using Physical Optimization Techniques {Lecture}
  - Incremental Compile Flow {Lecture}

DAY 4

- Objective 6
  - QoR Reports Overview {Lecture, Lab}
  - Reducing Logic Delay {Lecture}
  - Reducing Net Delay {Lecture}
  - Improving Clock Skew {Lecture}
  - Improving Clock Uncertainty {Lecture, Lab}
  - Intelligent Design Runs (IDR) {Lecture, Lab}
  - Introduction to Floorplanning {Lecture}
- Objective 7
  - Vivado Design Suite ECO Flow {Lecture, Lab}
  - JTAG to AXI Master Core {Lecture}
  - Trigger and Debug at Device Startup {Lecture}
  - Trigger Using the Trigger State Machine in the Vivado Logic Analyzer {Lecture, Lab}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works

    - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vivado 2022.2
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

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Qualiopi processus certifié
RÉPUBLIQUE FRANÇAISE
La certification a été délivrée au titre de la catégorie d'action suivante :
ACTIONS DE FORMATION