Vitis™ High Level Synthesis

COURSE DURATION

2 days - 14 hours

TARGET OBJECTIVES AND SKILLS

- 1 - Describe the high-level synthesis flow, use the Vitis HLS tool for a first project and identify the importance of the test bench
- 2 - Use directives to improve performance and area and select RTL interfaces
- 3 - Identify common coding pitfalls as well as methods for improving code for RTL/hardware
- 4 - Perform system-level integration of IP generated by the Vitis HLS tool

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.

PREREQUISITES

- C or C++ knowledge
- Basic knowledge FPGAs architectures

NOTES

- Release date: 15/11/2024

COURSE CONTENT

DAY 1

- Objective 1
  - Introduction to High-Level Synthesis {Lecture}
  - Vitis HLS Tool Flow {Lecture, Lab}
  - Vitis HLS Tool Command Line Interface {Lecture, Lab}
  - Introduction to HLS UltraFast Design Methodology {Lecture}
- Objective 2
  - Design Exploration with Directives {Lecture}
  - Introduction to I/O Interfaces {Lecture}
  - Block-Level I/O Protocols {Lecture, Lab}
  - Port-Level I/O Protocols {Lecture, Lab}
  - Port-Level I/O Protocols: AXI4 Interfaces {Lecture}
  - Port-Level I/O Protocols: Memory Interfaces {Lecture, Lab}
  - Pipeline for Performance: PIPELINE {Lecture, Lab}

DAY 2

- Objective 2
  - Pipeline for Performance: DATAFLOW {Lecture, Lab}
  - Optimizing Structures for Performance {Lecture, Lab}
- Objective 3
  - Vitis HLS Tool Default Behavior: Latency {Lecture}
  - Reducing Latency {Lecture}
  - Improving Area and Resource Utilization {Lecture, Lab}
  - Vitis HLS Tool C Libraries: Arbitrary Precision {Lecture, Lab}
  - Hardware Modeling {Lecture}
  - Using Pointers in the Vitis HLS Tool {Lecture}
- Objective 4
  - HLS Design Flow – System Integration {Lecture, Lab}

TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- **Teaching methods :**
  - Alternating lectures, technical questionnaires and exercises on individual machines.
- **Pedagogical follow-up :**
  - Signed attendance sheet
- **Pedagogical assessment :**
  - Continuous assessment and progress sheet :
    - Technical questionnaire
    - Practical work results
    - Validation of objectives
- **Satisfaction survey :**
  - At the end of training: assessment form completed by the trainee
  - At 3 months: evaluation form completed by the trainee after application to the company
- **Certificate :**
  - Training certificate with assessment of learning provided to trainee
  - Certificate of completion provided to employer

TEACHING METHODS

- **Inter-company online training :**
  - Fast Internet connection, webcam, headset
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on individual Cloud PC by RealVNC
- **Intra-company face-to-face training on customer site : (details to be confirmed prior to training)**
  - Suggested supply by the customer :
    - Training room
    - Video projector
    - Whiteboard
    - Individual PC with AMD tools
  - Provided by MVD Training :
    - Course material in PDF format
    - Practical work on individual PCs (loan of equipment available on request)

RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
  - Recent computer OS Linux or Windows 64-bits
  - Fast Internet, webcam, headset
  - Software tool WebEx Cisco
  - ***AMD remote tools :***
    - Software tool RealVNC Viewer
  - ***AMD local tools :***
    - Software tool AMD Vitis
- **Face-to-face training on customer site :**
  - Recent computer OS Linux or Windows 64-bits
  - Software tool AMD Vitis

TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

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