Workshop : Designing with the Network On Chip of AMD Versal (French Language) 9h - 17h CET

COURSE DURATION

1 day - 7 hours

TARGET OBJECTIVES AND SKILLS

- After completing this comprehensive training, you will have the necessary skills to:
  - Identify the major network on chip components in the Versal ACAP
  - Include the necessary components to access the NoC from the PL
  - Configure connection QoS for efficient data movement

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.

PREREQUISITES

- Any Xilinx device architecture class
- Familiarity with the Vivado® Design Suite

NOTES

- Release date: 15/11/2024

COURSE CONTENT

DAY 1

- NoC Introduction and Concepts
- NoC Architecture
- NoC DDR Memory Controller
- NoC Performance Tuning

TEACHING METHODS

- **Inter-company online training :**
  - Fast Internet connection, webcam, headset
  - Presentation by Webex by Cisco

RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
  - Recent computer OS Linux or Windows 64-bits
  - Fast Internet, webcam, headset
  - Software tool WebEx Cisco

TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

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