Designing with Versal™ AI Engine

COURSE DURATION

4 days - 28 hours

TARGET OBJECTIVES AND SKILLS

- 1 - Describe the Versal™ architecture and the complete application acceleration workflow with the Vitis™ tool.
- 2 - Describe the architecture and the memory access structure of the AI Engine
- 3 - Program a single AI Engine kernel using the Vitis IDE tool
- 4 - Program multiple AI Engine kernels using Adaptive Data Flow (ADF) graphs
- 5 - Utilize the AI Engine DSP library for faster development

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- People with disabilities may have special training needs. Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability. Don't hesitate to to discuss your requirements.

PREREQUISITES

- Comfort with the C/C++ programming language
- Software development flow
- Vitis software for application acceleration development flow

NOTES

- Release date: 09/05/2025

COURSE CONTENT

DAY 1

- Objective 1
  - Overview of Versal ACAP Architecture {Lecture}
  - System design flow {Lecture, Labs}
- Objective 2
  - Versal AI Engine Architecture {Lecture}
  - Versal AI Engine Memory and Data Movement {Lecture}
- Objective 3
  - Scalar and Vector Data Types {Lecture}
  - AI Engine APIs {Lecture, Lab}

DAY 2

- Objective 3
  - I/O Buffers and Streaming Data APIs {Lecture}
  - Design Analysis : Vitis Analyzer {Lecture}
  - The Programming Model: Single Kernel {Lecture, Lab}
  - Introduction to AI Engine APIs for Arithmetic Operations {Lecture}
  - AI Engine Kernel Optimization – Compiler Directives {Lecture}
  - The Programming Model: Single Kernel Using Vector Data Types {Lab}
  - AI Engine Symmetric and Asymmetric Filter Implementation {Lecture, Lab}

DAY 3

- Objective 3
  - AIE Kernel Optimization – Coding Style {Lecture, Lab}
- Objective 4
  - The Programming Model: Introduction to the Data Flow Graph {Lecture}
  - The Programming Model: Multiple Kernels Using Graphs {Lecture, Lab}
  - AI Engine Application Debug and Trace {Lecture}

DAY 4

- Objective 4
  - Advanced Graph Input Specifications {Lecture}
  - Graph Input and Runtime Parameters {Lecture, Lab}
- Objective 5
  - AI Engine DSP Library Overview {Lecture, Lab}
- Appendixes(optional)
  - AI Engine Symmetric Filter Implementation using Intrinsics {Lecture}
  - Introduction to the AIE-ML Architecture {Lecture}
  - AIE-ML Memory Tiles and Programming {Lecture, Lab}

TEACHING METHODS AND SUPPORT - ASSESSMENT & RECOGNITION

- **Teaching methods :**
  - Alternating lectures, technical questionnaires and exercises on individual machines.
- **Pedagogical follow-up :**
  - Signed attendance sheet
- **Pedagogical assessment :**
  - Continuous assessment and progress sheet :
    - Technical questionnaire
    - Practical work results
    - Validation of objectives
- **Satisfaction survey :**
  - At the end of training: assessment form completed by the trainee
  - At 3 months: evaluation form completed by the trainee after application to the company
- **Certificate :**
  - Training certificate with assessment of learning provided to trainee
  - Certificate of completion provided to employer

TEACHING METHODS

- **Inter-company online training :**
  - Fast Internet connection, webcam, headset
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on individual Cloud PC by RealVNC
- **Intra-company face-to-face training on customer site : (details to be confirmed prior to training)**
  - Suggested supply by the customer :
    - Training room
    - Video projector
    - Whiteboard
    - Individual PC with AMD tools
  - Provided by MVD Training :
    - Course material in PDF format
    - Practical work on individual PCs (loan of equipment available on request)

RECOMMENDED COMPUTER HARDWARE

- **Inter-company online training :**
  - Recent computer OS Linux or Windows 64-bits
  - Fast Internet, webcam, headset
  - Software tool WebEx Cisco
  - ***AMD remote tools :***
    - Software tool RealVNC Viewer
  - ***AMD local tools :***
    - Software tool AMD Vitis 2024.2
- **Face-to-face training on customer site :**
  - Recent computer OS Linux or Windows 64-bits
  - Software tool AMD Vitis 2024.2

TEACHING STAFF

- **William Duluc, Electronics and Telecoms Engineer, AMD Expert since 2009 and AMD Trainer since 2017 :**
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

TECHNICAL, EDUCATIONAL, ADMINISTRATIVE AND FINANCIAL CONTACT

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